WIDE BANDGAP SUPERLATTICE POWER DEVICES FOR ARMY HYBRID ELECTRIC POWER SYSTEMS

T. Burke*, G. Khalil, J. White
U.S. Army TARDEC
Warren, MI. 48397-5000

C.G. Wang
Nanodynamics-88, Inc.
New York City, NY. 10016-7918

K. Donegan
C9 Inc.
Kingston, NY 12401

D. Weidenheimer
L3 Pulse Sciences
San Leandro, CA 94577-5602

ABSTRACT

The size, weight, performance and thermal management of hybrid-electric power systems are limited by the performance of available silicon power devices. Potential improvements afforded by wide bandgap silicon carbide devices have been confirmed in Army programs, but the commercially available material severely limits performance. Superlattice silicon carbide material addresses the key limitations of this material; quality, size, cost, and incompatibility with silicon processing. Wide bandgap superlattice silicon carbide material has recently been grown on 4-inch diameter silicon substrates by NanoDynamics-88, Inc/C9 Corp

1. INTRODUCTION

Power devices made from silicon carbide offer a potential means to achieve the higher power density, improved efficiency, and reduced thermal management needed to integrate advanced electrical power systems in Army hybrid electric combat vehicles. This potential has not been realized because the material is too expensive, has a high concentration of defects, and is only available in sizes up to 4 inch diameter. In spite of considerable improvement in commercially available silicon carbide (SiC) materials, 3 inch diameter starting material costs approximately $10,000, and killer defect concentration is on the order of 5 cm^{-2}. As a result, only small low-current devices can be produced with an acceptable yield, and the cost precludes large-scale power switch commercialization. A novel material, superlattice silicon carbide (Si/C) has the potential to overcome all of these limitations. Commercially available 4H polytype silicon carbide (4H-SiC) is grown by physical vapor transport (PVT) at temperatures well beyond the melting point of silicon. In contrast, superlattice material is grown at low temperatures compatible with silicon processing, and can be grown on inexpensive large diameter silicon substrates.

2. ARMY HYBRID ELECTRIC APPLICATIONS

Hybrid electric architecture can provide combat vehicles with new capabilities such as extended silent watch, silent mobility, and the ability to generate hundreds of kilowatts of electrical power. This electrical power can be used on the vehicle for traction, survivability, electric guns, and directed energy weapons, or for off-vehicle applications, such as battery charging or supplementing electrical generators. High-power electrical power supplies, or "power converters", such as generator controllers, traction motors inverters, and battery pack dc-dc converters for charging/discharging, are required for all of these functions. Future vehicles may also require power converters for electro-magnetic armor, electric guns, and directed energy weapons such as lasers or high power microwave sources. It is also likely that power demands for sensors, communication, and computing will continue to increase.

Consequently, a key challenge for a hybrid-electric vehicle architecture, such as that adopted by FCS Manned Ground Vehicle, is to integrate these high power converters and meet their cooling requirements. For successful integration, the electrical power system

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
01 NOV 2006	**N/A**	**-**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
Wide Bandgap Superlattice Power Devices For Army Hybrid Electric Power Systems	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **U.S. Army TARDEC Warren, MI. 48397-5000**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release, distribution unlimited

13. SUPPLEMENTARY NOTES
See also ADM002075., The original document contains color images.

14. ABSTRACT

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**	**UU**	**8**	

Standard Form 298 (Rev. 8-98)
Prescribed by ANSI Std Z39-18

components must be compact and efficient, and place minimal burden on the vehicle cooling system.
Significant improvements in power converter power density and power/weight have been demonstrated in the last six years, as a result of intensive efforts in TARDEC ATO and ARL programs. Motor drive inverter and dc-dc converter power densities have been doubled. However higher power density, increased operating temperatures, and further improvements in efficiency are still needed to achieve the full capability of hybrid electric power systems, and transition them to Army systems.

In spite of the fact that existing silicon power electronics performs conversion very efficiently, typically 92-99 %, improvements in efficiency are still needed. In typical operation, a number of power conversion steps naturally occur in sequence, from power generation to energy storage to final use. The overall net efficiency after a sequence of conversions can be considerably lower, 80% - 95%. Further improvements in power converter efficiency are also needed because the 5 -20 % waste heat places an additional burden on the vehicle cooling system, and requires significant power for fans and pumps. At existing efficiencies, removal of the waste heat from a 350kW electrical system, including diesel-generator, requires on the order of 50kW.

Radiator size can be reduced by operating at higher coolant temperatures. Heat rejection is proportional to the coolant-to-ambient temperature difference. Consequently, a smaller radiator operating with higher temperature coolant can remove the same heat load as a larger radiator operating at lower coolant temperature. This effect can be significant, for example; by increasing coolant temperature from 65 ^{o}C to 80 ^{o}C, radiator size can be reduced by approximately 50% (based on rejection to a 50C ambient).

Silicon material and silicon processing technology is the gold standard of the semiconductor industry in performance and cost, but lacking a wide bandgap, silicon devices cannot function at elevated temperatures. Operation with even 80 ^{o}C coolant is not yet practical with conventional silicon IGBT devices. In general, silicon power devices can operate to maximum junction temperatures up to 150–175 ^{o}C. Good engineering practice derates this to about 85%, and manufacturers ratings are typically supplied at 125 ^{o}C. Given the relatively high thermal resistance of power module packages, this limits
coolant temperatures to about 65 ^{o}C. Silicon carbide devices can operate at much higher temperatures.

High frequency operation is a key strategy to increase power density and power/weight by reducing the size of magnetics and filter components. DC-DC converter input and output filters are smaller at high switching frequency. The effect is significant, for example at twice the frequency the same voltage ripple attenuation can be obtained using only half the inductance or half the capacitance. Higher frequency operation also acts to reduce inductor core losses and minimize required core size. Magnetic cores are sized to handle heat from core losses. These core losses are proportional to ac magnetic flux density. For a given rms voltage, higher frequency operation reduces ac flux density, and therefore reduces the core size required to handle the related losses. In practice however, parasitic losses associated with high frequency operation, such as skin effect, frequency-dependent ESR, and power device switching losses, limit operating frequency. The workhorse of Silicon power electronics is the IGBT. (insulated gate bipolar transistor). It is limited to operating at about 30 kHz, at high power in hard-switched mode. Silicon IGBTs designed to do this also have very high conduction losses. These high losses reduce efficiency. A hard frequency limit is reached when losses cause the device to reach the maximum allowable junction temperature of silicon, approximately 150 ^{o}C. Silicon carbide power devices have faster switching speeds, lower losses, and a higher allowable junction temperature – all favoring high frequency operation.

To meet power requirements for 22 ton hybrid electric combat vehicles, power modules are needed with high current ratings of 300-600A and voltage ratings of 1200-1400 volts. This high current rating is best met with larger semiconductor die (chip) sizes that can operate at > 100-200 amperes. Large, high-current silicon devices are readily available, because affordable, low-defect, high quality large-area silicon material (6”-8” diameter) is available. In contrast, only 4 inch diameter silicon carbide is commercially available, and it has a high concentration of defects.

Future pulse power applications, such as electro-magnetic armor and ETC guns, vary significantly in electrical requirements. In general, very high voltages and very high pulsed current levels are required. Electro-thermal chemical (ETC) guns, for example, nominally require operation at 10,000 volts and 100,000 amperes, or higher. Operation at 100 kA clearly requires large-area devices. Large diameter single-wafer silicon devices are readily available but, due to silicon’s high losses, limited current density, and low electric field limit, must be operated in series and parallel combinations. The net result is that the overall semiconductor switch assembly is too large. Tubes,

such as triggered vacuum switches, are used instead. Silicon carbide offers lower losses, higher current density, and operation at much higher electric field.

3. ADVANTAGES OF SILICON CARBIDE

This section describes the theoretical advantages and status of power devices made of commercially available 4H-SiC, and the significant, even essential, improvement offered by superlattice Si/C. Theoretically, the improved performance of silicon carbide devices is related to superior material properties. The most important are high critical electric field, and wide bandgap.

4H-SiC FET (field effect transistor) and 4H-SiC Schottky rectifier devices parallel better and show significantly faster switching than their silicon IGBT counterparts. This results in lower switching losses, lower conduction losses, and higher frequency capability. The high critical field of silicon carbide enables these devices to operate at the voltages and powers needed for Army hybrid electric vehicles. The critical field of 4H-SiC is an order of magnitude higher than silicon. The benefit of this higher critical field on efficiency is apparent from Baliga's figure of merit.

$$\mu_n \varepsilon_r \varepsilon_0 E_C^3$$

Where μ_N is mobility, ε_r is dielectric constant, ε_0 is permittivity, and E_C is the critical (avalanche) electric field. Baliga's figure of merit (Baliga, 1997) is inversely proportional to the specific on-state resistance of the drift layer of an FET or Schottky rectifier. Compared to silicon (1), silicon carbide has a value of 223. This allows a silicon carbide drift layer to have almost two orders of magnitude lower resistance than a silicon drift layer, designed to block similar voltage. This property allows a high voltage silicon carbide FET to operate more efficiently than a silicon IGBT.

The dependence of operating temperature on bandgap (Eg) can be estimated from the intrinsic temperature. The intrinsic temperature provides an absolute upper limit to high temperature operation. At this temperature, the concentration of thermally generated free carriers, n_i, becomes equal to the background concentration, typically $5x10^{14} - 5x10^{15}$ cm^{-3}, and semiconductor junctions lose voltage blocking capability. This temperature is proportional to the semiconductor bandgap (Sze, 1981) :

$$n_i = (N_C N_V)^{0.5} \exp(-Eg/2kT)$$

Silicon carbide's wide bandgap, Eg ~ 3 eV , allows silicon carbide devices to operate at much higher temperatures than silicon devices (Eg = 1.12 eV). NASA has demonstrated switching at 647 ^oC. Similarly, a bandgap-engineered superlattice Si/C material with a wide bandgap of only 2 eV would still be expected to operate at 254°C, including a 15% derating factor. This is a practical upper temperature limit as well, in that most insulating materials cannot sustain an operating temperature much beyond 250°C. The capability to operate at 250 ^oC junction temperature would enable the use of very high temperature coolant, and also reduces the need to derate devices for surge conditions, allowing smaller, cheaper devices.

4. LIMITATIONS OF COMMERCIAL SILICON CARBIDE

The combination of high material cost, limited substrate size, and the high concentration of defects in commercially available silicon carbide, makes devices very expensive. The cost of material s is on the order of $10,000 for a 3" diameter substrate wafer with epilayers. Consequently, in spite of their improved performance, no power switches are commercially available, except on a custom basis.

The high concentration of defects in conventional SiC limit device performance, reliability, yield, choice of device type, and, to an extent, device current rating.

As a semiconductor, SiC does not have a liquid phase to form a single crystal ingot like silicon except at 2,800°C and an extreme pressure. With a lattice matched template, SiC crystals can be grown with physical vapor transport at 1,800°C or with CVD at 1,600°C, but both thermal budgets are above the melting point of silicon (1,408°C). This high thermal budget in fabrication brings about the following problems:

- The SiC crystal is often covered with micro-pipe defects, which would short devices containing them. As a result, SiC devices are usually mm in size in order to avoid the micro-pipes.

- SiC can have crystal structures of 3C, 4H, 6H, 8H, 12H, 12R etc, with each having a different band-gap and thermal expansion coefficient. During high temperature fabrication, the Boltzmann factor allows most of these crystal structures to participate in equilibrium and their participation, or the polytype structure cannot be annealed away in order to obtain a low strain single crystal. Devices made from them must operate at much

lower temperature where the polytype material is greatly strained

- In addition to micropipes and polytype inclusions, high thermal budgets in fabrication creates many other defects such as massive dislocations, stacking faults, etc. Note that in the binary material SiC, carbon atoms do not move or diffuse except at temperatures above the melting point of silicon (thus vapor pressure and micro-pipes), and this is the principal difficulty of forming single crystals SiC with low defect density.

Micropipes are tubular voids formed from hollow-core dislocations. They extend along the c-axis growth <0001> direction. The presence of even 1 of these within a device, significantly degrades its voltage blocking capability. Unfortunately, they propagate from the substrate into the voltage-blocking epitaxial layers. Over the past 10 years, micropipe defect concentrations have been dramatically reduced from approximately 100/cm^2 (on 2" material) to approximately 5/cm^2 on commercially available 3 inch diameter material. Recent efforts have consistently demonstrated materials with average micropipe concentrations less than 5/cm^2. The conventional material growth method (Physical Vapor Transport) is also capable of producing very low micropipe material. A. Powell reported 3 inch material with an average micropipe density of 0.04/cm^2 at the 2005 ICSCRM. However, the micropipe concentration in commercially available material is still considerably higher. In order for the commercial PVT growth process to be commercially viable for high power devices, the low micropipe process must be transitioned to high-volume production.

A defect-related failure called "Vf drift", occurs in SiC PiN diodes (Stahlbush et al., 2002). It is due to stacking faults formed from basal plane dislocations, by means of a defect reaction that uses the recombination energy present in bipolar devices. It is evidenced by a large increase in forward voltage during operation. There is some evidence it is also responsible for current gain degradation observed in silicon carbide bipolar transistors. Cree Research has made significant progress in overcoming this, with an improved material growth process, and approaches to device fabrication that have a stabilizing effect (Palmour, 2005). However, the overall economics and transition of these approaches to large-scale production are not conclusively established.

SiC substrates are commercially available in 2", 3" and 4" diameters. The availability of 4" diameter material significantly reduces device cost. Device fabrication costs for 4" material are only incrementally higher than 3", but area is almost doubled. Unfortunately, due to difficulty in controlling growth conditions over the larger area, the micropipe density of commercially available 4 inch diameter material is high. Cree 4" diameter low-micropipe density grade material is specified at <15 /cm^2, in comparison to <5 micropipes/cm^2 for ultra-low micropipe density grade 3" diameter material.

5. SILICON CARBIDE DEVICE STATUS

Due to low losses, fast switching, and compatibility with existing silicon gate drives, 4H-SiC MOSFETs are expected to be the best device for Army continuous power systems and the first device to be commercially available. MOSFETs with low specific on-state resistances have been demonstrated. Cree Research reports 1800V 4H-SiC MOSFETs with a specific on-resistance of 8 milliohm-cm^2 (Palmour et al., 2005). However, at present, 4H-SiC MOSFETs have severe limitations with respect to channel mobility, threshold (control) voltage stability, and gate dielectric reliability. All of these limitations are related to high interface defect concentrations. Superlattice material offers the possibility of a low defect oxide-semiconductor interface. Superlattice Si/O has been grown on silicon with low defect density.

Low resistance (6.68 milliohm-cm^2) 4H-SiC Schottky rectifiers with voltage ratings required for Army systems (1789V) have been demonstrated (Zhao et al., 2004). 4H-SiC Schottky rectifiers are commercially available in large quantities form Cree Research, Inc. and Infineon. Unfortunately, due to 4H-SiC material quality, it is only available at ratings up to 20 amperes.

The benefit of thinner, lower resistance blocking layers extends to 4H-SiC Bipolar Junction Transistors (BJTs) and bipolar "PiN" diodes. These bipolar devices have advantages over the MOSFET and Schottky rectifier with respect to low forward voltage drop at very high voltages (> 3 kV), very high temperatures (> 250 ^{o}C) and very high current density (> 400 A/cm^2). These characteristics make them well-suited for pulse power and utility applications. The SiC BJT is also a potential candidate for a near-term high power silicon carbide switch. The lowest specific on-state resistance yet demonstrated for a high voltage (727V blocking) BJT is 2.9 milliohm-cm^2 (Zhang et al., 2006). SiC PiN diodes have demonstrated the very high voltages (10 kV) needed for pulse power application (Palmour et al., 2005).

In general, silicon carbide's properties are uniquely suited for pulse power applications (Burke et al., 1997). At present, conventional silicon carbide material is not suitable for large-area, > 10 cm^2, or whole-wafer pulse power devices due to a high concentration of defects called "micropipes".
In addition, the performance and availability of BJTs and PN diodes for both continuous and pulse applications may be severely limited by Vf drift. (Stahlbush et al., 2002). For pulse power, this is compounded by the possible generation of additional defects from the thermo-mechanical stresses that occur during pulse power operation. Superlattice Si/C material offers significant advantages over commercial material for pulse power. It does not have micropipes. On the near term, very large single-wafer devices are possible. Nanodynamics-88/C9 Inc. has built a growth reactor for 6 inch diameter material. Low defect 6 inch diameter material grown by the commercial PVT process will not be available in the foreseeable future. Pulse power Superlattice Si/C devices will have to demonstrate low-loss vertical conduction, or demonstrate some other method for achieving the required high voltage holdoff.

Conventional 4H-SiC is an important part of the Army's hybrid electric power systems development.
Based on theoretical considerations and prototype device demonstrations, silicon carbide power systems are estimated to be 1/3 the size of conventional silicon power electronic systems, and capable of operating above 100 ^oC. However, the high concentration of defects in the conventional SiC starting material significantly limits performance and availability of all SiC devices. Superlattice silicon carbide with its much reduced defect density, offers a potential solution.

6. FABRICATION AND PROPERTIES OF SILICON-BASED SUPERLATTICES Si/O AND Si/CO, AND Si/C

The primary objective of this paper is to present the status and potential of superlattice Si/C.
Si/O and Si/CO are discussed because the growth technique for Si/C emerges from superlattice Si/O. Superlattice Si/O may also be used to complement and enhance the capabilities of Si/C, by providing a superior replacement for SiO_2 for SOI, MOSFET gate dielectric, or passivation.

R. Tsu proposed in 1993 a silicon-based strain layer superlattice (Tsu, 1993) where non-silicon atoms would compound with silicon, atomic layer by atomic layer, to form silicon compound with band-gap engineered materials. He assigned the development task to NanoDynamics, Inc. During the past 12 years, with many rounds of SBIR Phase I and Phase II, plus several subcontracts for ITP (integrated product teams) supported by DMEA and TARDEC of the Army, the following superlattice properties have been firmly established:

- The superlattice Si/O can be constructed with very low strain (≤1%) and very low interface defect density (~10^8-10^9/cm^2) and function as a high quality epitaxial insulator on silicon. This epi-Si/O can support SOI (silicon-on-insulator) wafer construction with the exceedingly thin top epi-layer being grown, instead of shaving off from the bonded top layer as practiced by the bonded wafers approach. The epi-insulator for SOeI (semiconductor on epi-insulator) can be particularly useful for ultra-ultra thin top device layers for radiation immune designs and can also serve the 3-D chip architecture.
- Si/O and Si/CO superlattices exhibit direct band-gap characteristics as shown in photo-luminescence (PL), with Si/O peaking at 2.1eV and Si/CO peaking at 2.2eV (Tsu, 2005). The measured PL for Si/O and Si/CO are bright and highly efficient.
- From the epi-Si/O insulator, it is possible to grow an epi-Si/C superlattice for device construction so that the devices fabricated from the SOeI wafers can survive very wide temperature swings. The wide band-gap Si/C being grown on the insulating Si/O substrate is a new material that can use silicon processing to carry out device fabrications.

7. CONSTRUCTION OF Si/O SUPERLATTICE

The Si/O superlattice is described in depth in chap. 6 of Superlattice to Nano Electronics (Tsu 2005).
Most silicon devices require an insulation layer of SiO_2 constructed upon the silicon matrix.
But with 38% lattice mismatch, SiO_2 grown on Si for more than a few atomic layers is necessarily amorphous. Using silicon wafers for devices, the silicon surface is typically first treated with HF acid to remove much of the native surface oxides and engage the surface with dangling hydrogen atoms. At a slightly elevated temperature (~400°C), the hydrogen atoms will form H_2 gas and leave under vacuum. The nearest silicon surface bonds will form dimers at ~600°C with a binding energy of 225 kJ/mole. The dimers will now effectively seal the surface against most surface chemistries at low temperatures. O_2 gas can be ionized in atomic form with 498 kJ/mole. By

introducing O_2 to the dimers, the O_2 is energetically favored to break up and couple with the dimers because the two Si-O bonds with 800 kJ/mole are higher than the dimer (225) plus the O_2 (498) bonds. The oxygen atoms will now be dangling on the surface, just like the dangling hydrogen atoms. This structure is easily verified from RHEED (reflection high energy electron diffraction) images in real time in MBE. At low temperatures, this surface oxidation is self-limiting because the reaction is specific to the dimers, and will terminate as soon as all the surface dimers are used up. A new layer of silicon deposition on the surface with dangling oxygen would immediately form a new dimered silicon surface. Figure 1 is the TEM view of the Si/O superlattice where the interface strain has propagated up to ~5 atomic layers, and the lattice mismatch is ≤1%. Because of this very low strain, the Si/O superlattice will exhibit virtually the same high quality epitaxy at the 100th period as that of the first period on the epi-silicon surface.

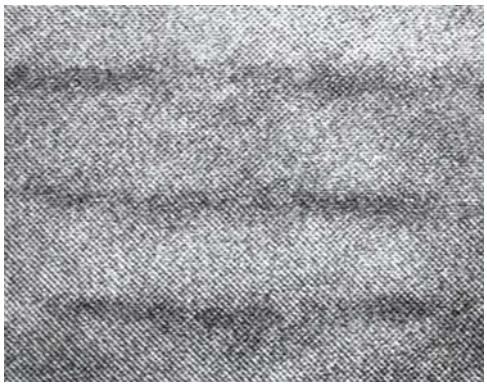

Figure 1: Si/O superlattice (Tsu, 2005)

While silicon does not have a direct band-gap for efficient optical transitions, the superlattices Si/O and Si/CO do, because their unit cell in k-space is much reduced and therefore aligned for direct optical transitions. Figure 2 shows the photo-luminescence of Si/CO and Si/O. The emissions are quite bright.

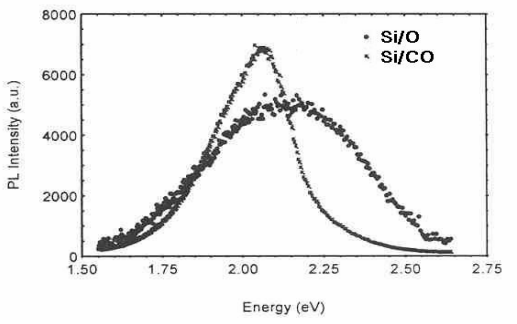

Figure 2: PL of Si/O and Si/CO superlattices (Tsu, 2005)

8. Si/C SUPERLATTICE

Carbon does not move in the silicon matrix except at very high temperature. We, however, have already constructed the Si/O superlattice with low defect density. Therefore on the oxygenated silicon surface, (not SiO_2 surface), each dangling oxygen provides a lattice site to attach to carbon-containing molecules. The carbon-containing source molecules were selected with pre-assembled carbon/silicon binding, the proper σ bond, and with many surrounding hydrogen atoms so that they can readily leave and allow the C/Si molecules to be ionized and attach to the dangling surface oxygen. As oxygen would bind on a silicon dimer at low temperature, it is self-limiting, therefore the carbon-containing molecules attaching to the dangling oxygen is also self-limiting. This makes the fabrication process relatively easy and low cost. In addition, while carbon atoms do not diffuse in the silicon matrix, oxygen ions would readily diffuse under silicon-processing temperatures and form O_2 gas, which will leave the surface under vacuum

Since the silicon and carbon layers are alternatively placed (lattice layer C-B-A-B-C, with A the silicon buffer layer providing a mirror-image between the template layers B and C beneath and the nascent layers C and B), whose ordering is similar to the conventional 4H-SiC, we therefore consider the new superlattice Si/C as the 4H structure (Figure **3).**

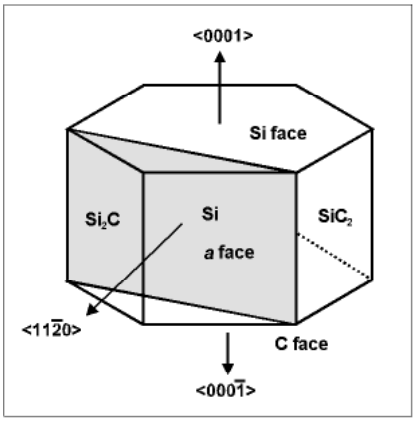

Figure 3: SiC structure

9. LATTICE MATCHED Si/C ON Si<100> AND Si<111>

SiC lattice dimension is ~20% smaller than silicon, so that a Si/C superlattice fabricated on the silicon template cannot be maintained epitaxially for more

than 4 or 5 atomic layers as we have observed from RHEED images. The layered superlattice structure alternating between Si layer and C layer largely avoids this difficulty except that the ratio of C/Si is much reduced from the conventional SiC at 50/50.

10. SUPERLATTICE MATERIAL PROPERTIES

Based on its low temperature fabrication and well-controlled growth, superlattice Si/C has fundamental advantages with respect to low defects, absence of micropipes, large area, and high crystal quality. To realize its full potential, the material must maintain high mobility, acceptable free-carrier lifetime, and high crystal quality across the larger area silicon substrate. Like conventional SiC, it must demonstrate the doping and layer thickness required, and doping and thickness uniformity. As with any emerging material, it will take time to determine all of its relevant properties. To provide proof of concept, the TARDEC BAA program with Titan/Nanodynamics-88 is following a direct strategy by demonstrating a high voltage Schottky device and extracting approximate parameters from device measurements. Results so far are very encouraging, with respect to doping level and control, wide bandgap, and Mobility.

Figure 4 shows the SIMS (secondary ion mass spectroscopy) data of an Si/C sample N^+ (Nitrogen containing) doping where the dopant molecules are woven into the source molecule in order to achieve an extremely high doping concentration while retaining the epitaxy in high quality.
Note that this Si/C superlattice follows the silicon surface template with silicon lattice dimensions. The nature of the growth process allows the dopant concentration to be easily controlled, by dilution of dopant gas sources

A wide bandgap property is suggested from the similarity of the structure of superlattice Si/C material to the structure of wide bandgap 4H-SiC. The capability of varying the carbon to silicon ratio offers the possibility of adjusting the bandgap.

Breakdown voltages are usually easily measured, but with superlattices constructed atomic layer-by-atomic layer, with each period at ~nm thick, a usual thin electrode coated on the material would already have a thickness equivalent to thousands of superlattice periods. The current fabrication instruments are still struggling to make only a few dozen periods each time.

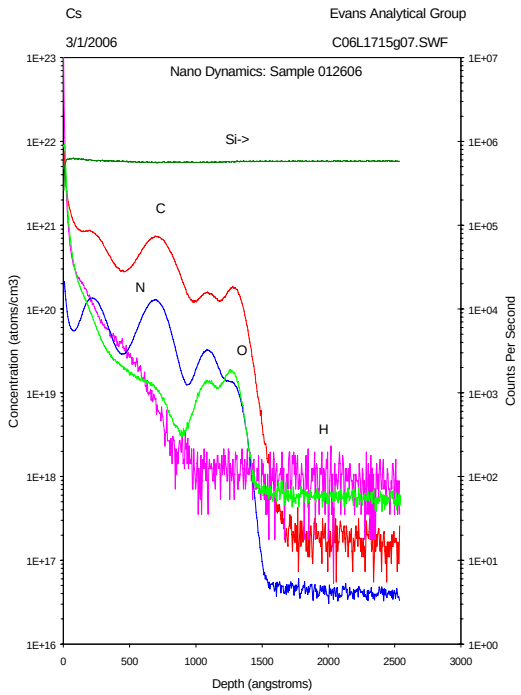

Figure 4: SIMS on n+ Si/C sample

Until our next generation processing instrument for superlattice construction becomes operational, we are limited to handle only extremely thin samples and must estimate certain performance parameters without experimental verification. The estimate of breakdown voltage (by R. Tsu, private communication) is a case in point. For an electron in a field E, the maximum energy it may gain, Eg, is:

$$E_g = \frac{1}{2} m v_m^2 \qquad or \qquad v_m = (\frac{2E_g}{m})^{\frac{1}{2}} = \mu E_m$$

With μ the mobility; μ=eτ/m and τ the carrier time,
E_m the maximum electric field. The maximum voltage $V_m=E_m\ell$, with ℓ the mean-free-path

$$\ell = \frac{V_m}{E_m} = v_m \tau \qquad i.e.,$$

$$v_m = (\frac{2E_g}{m})^{\frac{1}{2}} = \mu E_m = \frac{E_m e\tau}{m} = \frac{E_m e\ell}{v_m m} = \frac{V_m e}{v_m m}$$

so that $eV_m \sim 2E_g$.
Now an estimate of E_g (Si/O). For silicon, ΔE_c=0.92eV, ΔE_v=4.27eV, and E_g(Si)=1.12eV; therefore E_g(Si/O)=0.92+4.27+1.12=6.31eV.
Consider the unit cell structure quantum mechanically, the Si/O unit cell is twice in order to have the k-space at one-half as indicated by the direct optical transitions.

The E_g(Si/O) should therefore be reduced by ½, which makes it also close to the measured photo-luminescence value:

$$\frac{E_g(Si/O)}{E_g(SiO_2)} = \frac{3.15}{9} = 0.35 = \frac{V_M(Si/O)}{V_M(SiO_2)}.$$

Here $V_M(Si/O_2)=10^7$V/cm and V_M(Si/O)~3.5MV/cm, values similar to SiC and GaN.

Breakdown current flow is caused by the resistive thermal run-away causing often an irreversible change. But what initiates the breakdown is not thermal, rather it is the Zener tunneling where electrons are put into the conduction band, and the avalanche multiplication of the e-h pairs that gives a rapid increase of the carriers. Usually the avalanche phenomena would dominate over the Zener tunneling by far.

For Si/C epitaxially constructed on Si/O insulating substrate, Dr. William Mitchel of WPAFB did a Hall cross measurement and obtained a value $\mu \approx 1{,}100$ cm^2/V·sec. (This measurement was necessarily performed on structure with few Si/C layers, and will be confirmed when thicker material is produced using the new reactors). The theoretical value of SiC mobility μ is estimated at 700-750cm^2/V·sec for 3C or 4H. Another input on the mobility enhancement is to place large strain to the lattice. Silicon/Germanium superlattice, for example, forces the Ge lattice dimension on silicon and obtains an enhanced Si mobility of 35% higher, and upon which IBM recently announced that a world record of MOSFET speed at over 300GHz has been realized.

11. HIGH TEMPERATURE, HIGH FREQUENCY Si/C DEVICES

Unlike conventional SiC, the Si/C superlattice surface can be constructed with either Si or C, allowing construction of a pure silicon surface. A pure silicon surface can form contacts such as silicide or metal coating using aluminum plus gold, for example. In fact, much of the silicon-based technology like the use of copper interconnects can be adopted in this Si/C superlattice

Single devices such as Schottky diodes, IGBTs, etc. can readily be constructed on the Si/C wafers much like for pure silicon devices. This capability may be extended to include IC fabrication on the rad-hard SOeI (semiconductor on epi-insulator) wafers using Si/O. Using Si/C for ICs, they could serve high frequency responses because of the anticipated high "figure-of-merit", although we will operate the device much slower in order to achieve the radiation immune.

The ideal situation is to simply use silicon processing on silicon-like materials with wide band-gap so that devices can provide both the wide band-gap qualifications for high temperature operations yet are still under the well established design routines of silicon. This is the opportunity; a paradigm shift if realized.

REFERENCES

B. J. Baliga, 1997: Modern Semiconductor Device Physics, chap. 4, Power Devices, New York, Wiley.

T. Burke et al., 1997: Silicon Carbide Thyristors for Electric Guns, IEEE Trans. Magnetics, **33**, 432-436.

S. Dhar, et.al., 2005: Interface Passivation for Silicon Dioxide Layer on Silicon Carbide, MRS Bulletin, **30**, 288-292. (Zolper and M. Skowronski guest Editors)

D. Nakamura et al., 2004: Ultrahigh-quality silicon carbide single crystals , Nature,**430**, 1009-1012.

J.W. Palmour et al., 2005: Large Area Silicon Carbide Power Devices on 3 inch wafers and Beyond, CS ManTech 2005 Digest.

R.E. Stahlbush et al., 2002: Stacking Fault Formation in 4H SiC PiN Diodes, J. Elec. Mat., **31**, 370-375.

S. M. Sze, 1981, Physics of Semiconductor Devices 2nd Ed., chap.1,, New York, Wiley.

R. Tsu, 1993: Strain-Layer Silicon Superlattice, Nature, 19, 364.

R. Tsu, 2005: Superlattice to Nanoelectronics, Elsevier, London.

J. Zhang, P. Alexandrov, T. Burke, J. H. Zhao, 2006: 4H-SiC Power Bipolar Junction Transistor With a Very Low Specific On-Resistance of 2.9 m-ohm cm^2 , IEEE Elec. Dev. Lett. , **27**, 368-370.

J. Zhao et al.: 2004: Demonstration of 1789V, 6.68 milliohm-cm^2 4H-SiC merged-PiN-Schottky diodes, Electronics Letters, 40, 390-391